IN THE CLAIMS

Please amend claims 1, 5, 8, 11, 15 and 18 as follows:

1. (Previously Presented) A method of designing a video signal processing integrated circuit (IC), comprising the steps of:

providing the video signal processing IC with ~~having~~ an envelope detector for detecting and outputting an envelope of a frequency modulated (FM) video signal; ~~wherein:~~

providing the video signal processing IC with a level variation switching circuit for changing an envelope level of the FM video signal ~~according to an execution mode is incorporated into the video signal processing IC;~~ and

connecting an input of the level variation switching circuit to a control output of a microprocessor so that ON/OFF switching control of the level variation switching circuit is executed in response to a control data input from [[a]] the microprocessor.

2. (Original) The method according to claim 1, wherein the level variation switching circuit reduces variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in the control data input from the microprocessor.

3. (Original) The method according to claim 1, wherein the level variation

switching circuit operates in dependence on a playback mode of a video cassette recorder.

4. (Original) The method according to claim 1, wherein the level variation switching circuit has a resistor at an output terminal of the envelope detector.

5. (Previously Presented) A video signal processing integrated circuit (IC) incorporating an envelope detecting circuit for detecting an envelope level of an FM video signal, wherein the envelope detecting circuit comprises:

a peak detector for receiving the FM video signal and for detecting a peak value of the FM video signal; and

a level switch having a first input connected to an output of the peak detector and having a second input connected to a control output of a microprocessor for controlling the envelope level of the FM video signal according to mode information applied from [[a]] the microprocessor so as to reduce a variation in the envelope level in accordance with a type of mode of operation of a video cassette recorder (VCR).

6. (Original) The video signal processing IC according to claim 5, further comprising an amplifier connected to an input terminal of the peak detector for amplifying the FM video signal with a predetermined gain prior to provision to the peak detector.

7. (Original) The video signal processing IC according to claim 5, further comprising an amplifier connected to an output terminal of the peak detector for amplifying the FM video signal with a predetermined gain after processing in the peak detector.

8. (Previously Presented) [[The]] A video signal processing ~~IC according to claim 5,~~ integrated circuit (IC) incorporating an envelope detecting circuit for detecting an envelope level of an FM video signal, wherein the envelope detecting circuit comprises:

a peak detector for receiving the FM video signal and for detecting a peak value of the FM video signal; and

a level switch connected to an output of the peak detector for controlling the envelope level of the FM video signal according to mode information applied from a microprocessor so as to reduce a variation in the envelope level in accordance with a type of mode of operation of a video cassette recorder (VCR);

wherein the level switch includes a resistance element having a first terminal connected to the output of the peak detector and having a second terminal, and a switching control element connected to the second terminal of the resistance element, the switching control element being controlled by the mode information from the microprocessor.

9. (Original) The video signal processing IC according to claim 8, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.

10. (Original) The video signal processing IC according to claim 5, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.

11. (Previously Presented) A method of designing a video signal processing integrated circuit (IC) having an envelope detector for detecting an envelope of a frequency modulated (FM) video signal, said method comprising the steps of:

providing a level variation switching circuit in the video signal processing IC for changing an envelope level of the FM video signal according to an execution mode;

connecting an input of the level variation switching circuit to a control output of a microprocessor; and

providing an ON/OFF switching control of the level variation switching circuit in response to a control data input from [[a]] the microprocessor, said control data input containing playback mode information relative to the FM video signal.

12. (Original) The method according to claim 11, further comprising the step of providing the level variation switching circuit with a capability of reducing variation in the envelope level of the FM video signal according to standard playback (SP) mode information and super long playback (SLP) mode information, respectively, contained in

the control data input from the microprocessor.

13. (Original) The method according to claim 11, wherein the level variation switching circuit operates in dependence on a playback mode of a video cassette recorder.

14. (Original) The method according to claim 11, wherein the level variation switching circuit has a resistor at an output terminal of the envelope detector.

15. (Previously Presented) A video signal processing circuit for detecting an envelope level of an FM video signal input thereto, said circuit comprising:

peak detector means for receiving the FM video signal and for detecting a peak value of the FM video signal; and

level switch means connected to said peak detector means for controlling the envelope level of the FM video signal according to playback mode information relating to a mode of operation of a video cassette recorder (VCR), said playback mode information being applied ~~thereto~~ to said level switch means so as to reduce a variation in the envelope level in accordance with [[a]] the mode of operation of [[a]] the video cassette recorder (VCR).

16. (Original) The video signal processing circuit according to claim 15, further comprising an amplifier connected to an input terminal of said peak detector means for

amplifying the FM video signal with a predetermined gain prior to provision to said peak detector means.

17. (Original) The video signal processing circuit according to claim 15, further comprising an amplifier connected to an output terminal of said peak detector means for amplifying the FM video signal with a predetermined gain after processing in said peak detector means.

18. (Previously Presented) [[The]] A video signal processing circuit ~~according to claim 15,~~ for detecting an envelope level of an FM video signal input thereto, said circuit comprising:

peak detector means for receiving the FM video signal and for detecting a peak value of the FM video signal; and

level switch means connected to said peak detector means for controlling the envelope level of the FM video signal according to mode information applied thereto so as to reduce a variation in the envelope level in accordance with a mode of operation of a video cassette recorder (VCR);

wherein said level switch means includes a resistance element having a first terminal connected to said peak detector means and having a second terminal, said level switch means further including a switching control element connected to the second terminal of the resistance element, the switching control element being controlled by the

mode information applied to said level switch means.

19. (Original) The video signal processing circuit according to claim 18, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.

20. (Original) The video signal processing circuit according to claim 15, wherein the mode information comprises SP/SLP mode information relating to operation of the VCR.